MARTIN COMPANY
Electronics Engineering and Manufacturing

Clear Schematics

Clear Schematics.docx Revision 04 by John Martin 8 February 2017

Introduction: Clearly drawn schematics do a good job of communicating how electronic circuits work. It is worth the investment to draw schematics clearly so that design and peer reviews can explain and verify circuit operation. Typical customer team members who need to understand a set of schematics may include the electrical engineer, marketing engineer and project manager. Design team members who need to understand schematics may include the eCAD designer doing the PCB layout, software engineer writing firmware for the hardware, test engineer designing testing for the product, engineering managers who need to evaluate and have some control over the quality of the design, and peer engineers that review the design. Some projects at Martin Company require as many as 10 people to review or reference schematics before we build prototypes. Correctly drawn schematics in modern eCAD systems generate accurate BOMs and netlists for PCB layouts which greatly improves the efficiency and quality of output of electronics design projects.

Schematic Economies: We often describe a typical timeline and budget for a small project design phase as follows:

1) Schematics – 1 week or 6.7 %
2) PCB Layout – 2 weeks or 13.3 %
3) Firmware – 12 weeks or 80 %

Schematics can and should be a great driver for both hardware and software on most electronics projects. If they can be done correctly in the first 6.7 % of a project design phase and approved by the customer then the rest of the project is more likely to be done correctly and efficiently. Review of complete and correct schematics reduces project risk by getting early feedback from the customer and project team listed above. Even assuming a well done design specification, it is common for the schematics to be passed back and forth between the engineer/designer and the customer a number of times to finalize the details in order to meet customer requirements.

Figure 1 shows a typical change in cost for fixing a design flaw as the project moves through the phases. Schematics would normally be done during the design phase and the cost of finding and fixing a design flaw there can be as much as X100 lower than during production. Finding flaws early represents an enormous saving to the customer.

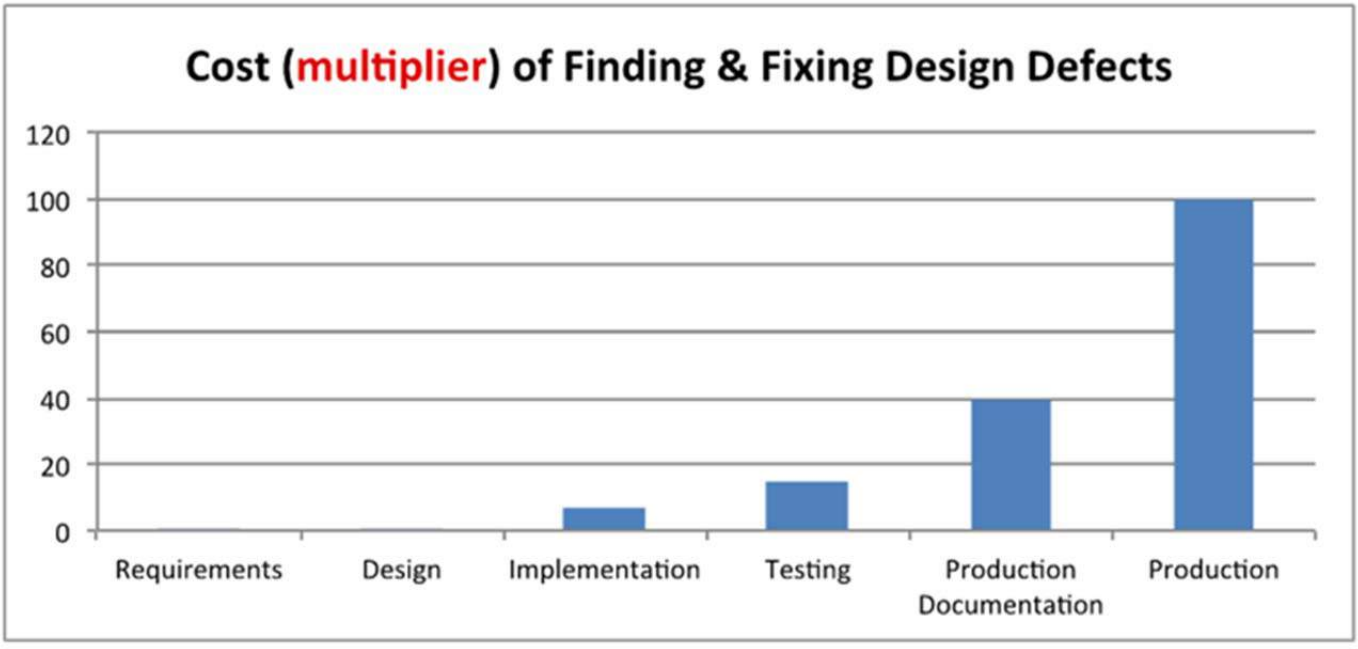


Figure 1 – Error Cost Escalation through the Project Life Cycle

Reference on slide – IBM Systems Sciences Institute, “Error Cost Escalation through the Project Life Cycle” by NASA for hardware and software and by Boehm in “Software Engineering Economics” 1981 for software alone.

Title Blocks, Revision Blocks, Notes: Title blocks should always include the name of the schematic or product, company name of the owner of the schematics, the name or initials of the person drawing the schematics, the date of the schematics last revision, revision number, and name or initials of design reviewer. Title blocks are normally the first item read on a drawing to provide context for the reader based on who did the design. In drawings that affect public safety title blocks are considered so important that the professional engineering seal and stamp are normally placed adjacent to them. Furthermore, a correctly filled in title block like Figure 2 helps identify the state of completion of schematics.

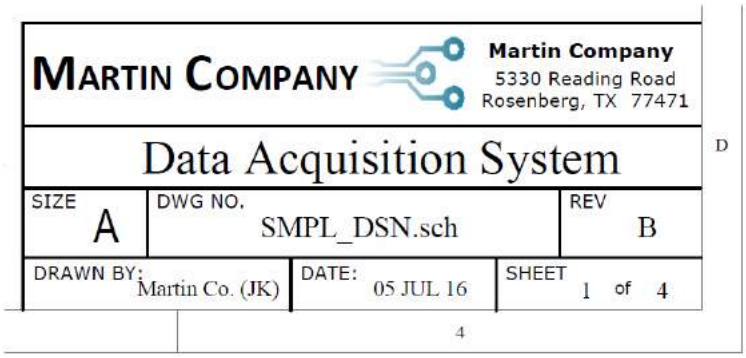


Figure 2 – Title Block

Normally our customer’s logos are shown in the title block instead of the examples with the Martin Company logo.

Notes should be located on the same page as the circuits that they describe so that they can be easily referenced. Some typical notes are shown in Figure 3.

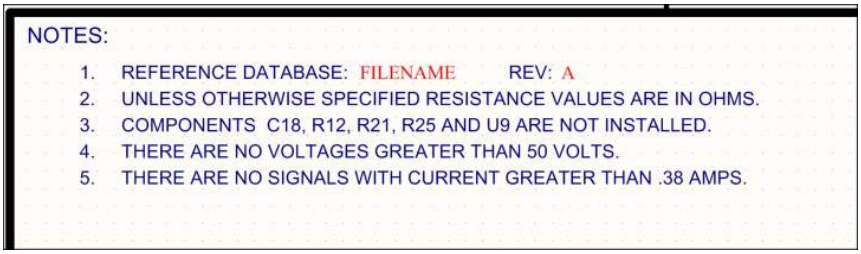


Figure 3 – Note Section

Revision blocks clarify the history of schematics and should include the revision number, description of revision, revision date, revision author, and revision approval. An example is shown in Figure 4 and on page 1 of the schematics at the end of this article.

Schematics Revision History					
ECN #	**Date**	**Initiated by:**	**Revised by:**	**Description**	**Approved**

Figure 4– Typical Revision Block

Title block, revision history and notes communicate who is responsible for the design and the history of the design. That context is also important to properly evaluate the design itself.

Page Breakdown: When a multipage schematic opens with a functional block diagram of a system design it helps clarify and summarize the design quickly. The first page often will show a hierarchical block diagram of the system as shown in Figure 5, and connectors and may show power supply connections. Schematics may also break up into analog signal conditioning, A/D, microcontroller + memory; display and power supply pages as shown in the example in Figure5.

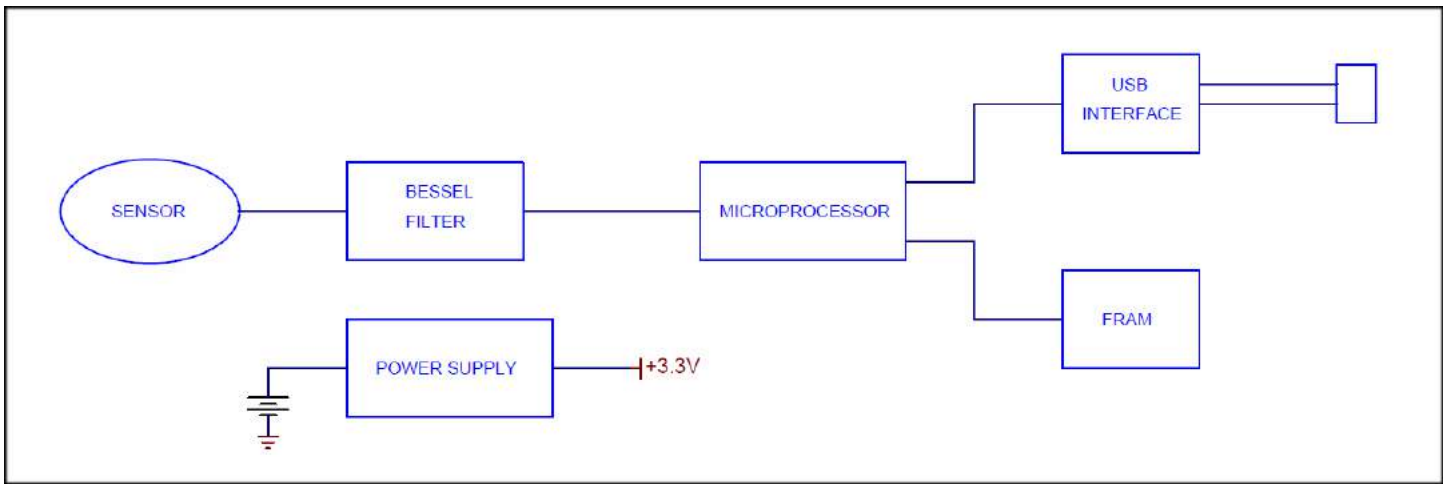


Figure 5 – Typical Block Diagram

Circuit Flow on Page: The signal flow should be from left to right and then circuit sections in order going down the page. Please refer to manufacturer's data sheets and application notes for good reference schematics. Lay out the schematics so that the operation of the circuitry is clarified. Figure 6 is an example of a power supply with AC transformer, rectifier and capacitors centered, and the 5 volt and 12 volt output regulators symmetrically arranged to the right. You can quickly see that the transformer, rectifier and capacitors are powering both regulators.

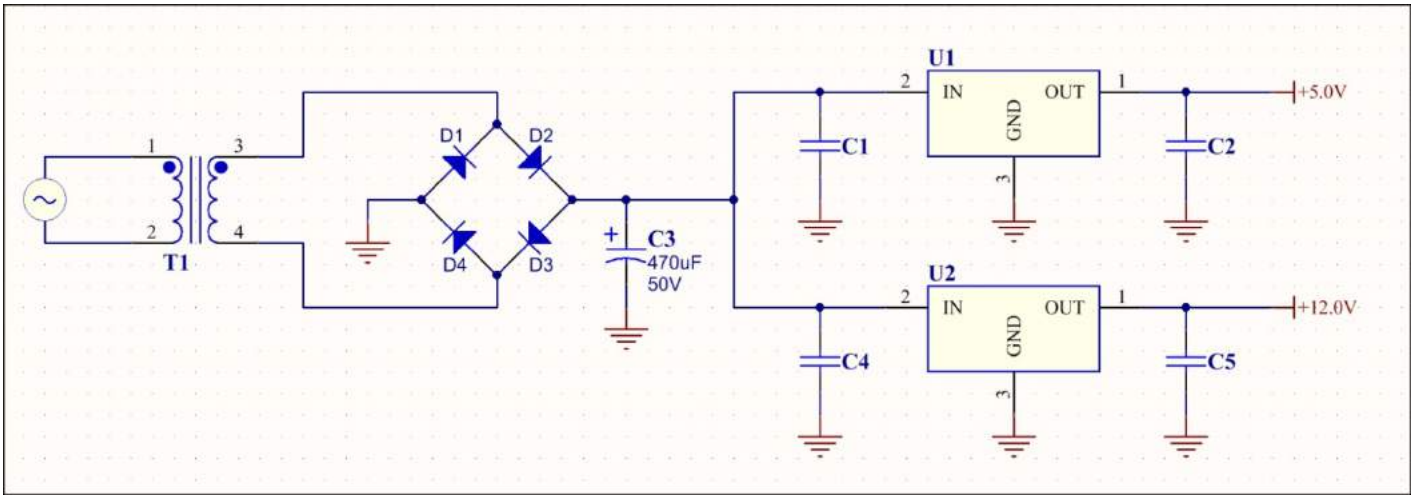


Figure 6 – Circuit Layout Example

In the 4KBIT EEPROM circuit shown in Figure 7, the SDO1 output is on the same side as the SDI1 input. In this case it is more important to show all of the SPI Bus lines together than to follow the inputs on the left and outputs on the right standard. This is really a judgement call on flow vs grouping for readability. For example if the page had a 100 pin processor on it, it might make more sense to group all the EEPROM communications and control lines for a single EPROM chip together on the processor instead of using the left/right scheme. When writing code or debugging a peripheral's firmware, the software engineer will be focusing on the pins for that peripheral, and if they are grouped together it may be easier to find the signals of interest than to follow the rule of inputs on the left and outputs on the right. For example, it would be poor design to show an input signal for chip X on the upper left-hand corner of a CPU and also show chip X output signals coming out the lower right-hand corner of the CPU.

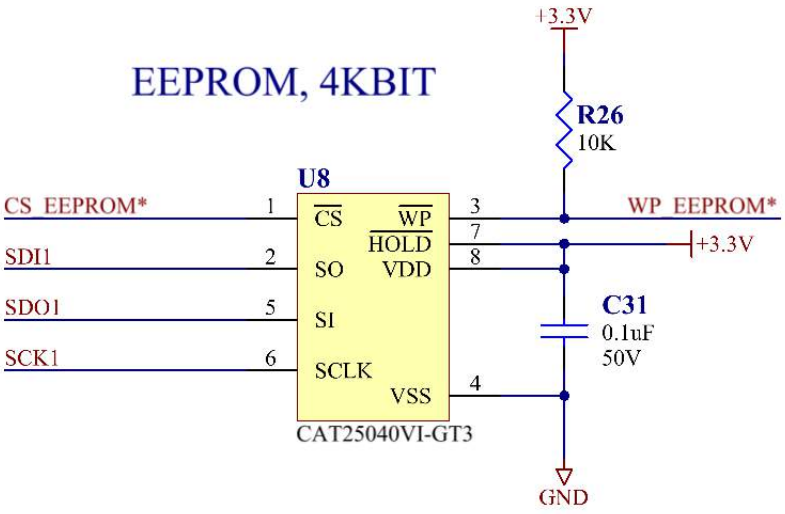


Figure 7 – 4KBIT EEPROM circuit

If signals are logically grouped together by functionality then it is important that the pin order be intuitive. For example, if several GPIO lines are used for a common purpose then the pins should be sequential bits of a common port. It is much easier for the firmware engineer to control digital channel lines if the lines are bits 0 though x on a common port as shown in Figure 8.

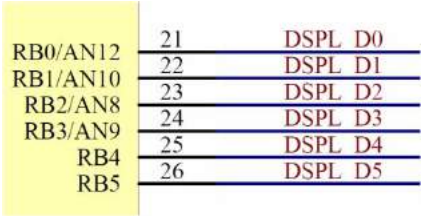


Figure 8 – Sequential Bit Order

Multifunctional pins on a component symbol should be labeled with all possible functions that pin supports as shown in Figure 9. The net names will then include the corresponding functions to be used. This is very helpful to the firmware engineer since data sheets for processors almost always refer to pins by several different names depending on the function. For example, if a pin corresponds to an I^2C module but is being used as a simple GPIO pin then the firmware engineer must ensure that the I^2C module is disabled.

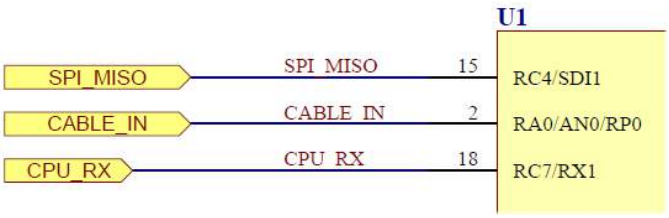


Figure 9 – Multifunctional Pin Labels

Component and Line layout: The ideal density for schematics can be determined by functional block diagram flow. If the circuit flows left to right and from top down, one or two signal flows may be all that you can get on an 11X17 drawing. By circuit or signal flow, we mean a section of circuit with an input and output that can stand on its own and be explained as having a particular functionality. This is affected by component size and components might be compared to an op-amp that is 0.75" tall on an 11X17 drawing having fonts of size 11 and above. It is preferable to use more sheets rather than to crowd components or circuit or signal flows. Proper use of white space on the page can improve the clarity and readability of schematics and also can make changes much easier. Clear schematics require thinking through how to best separate and compartmentalize circuit functions.

If a processor or FPGA has a large pin count it might be appropriate to split the IC into multiple subcomponent symbols to maintain proper white space for readability. For example, a processor with more than 100 pins may be broken into several symbols based on functionality like power, digital, and analog signals. These subcomponent symbols may then be placed on the pages with the corresponding functional components.

Net and Port names should be brief, intelligent descriptions, use underscores not spaces and begin with "N" or end with "*" for active low digital signals. Notes written into schematics in plain text should be used liberally especially in the early phases of a project when there may be a number of people who need to understand the design. See 4 pages of schematics at the end of this document for examples.

Lines that cross without connecting should include the crossover bump to be more explicit. Lines that do connect should be designated with dots.

Component Design and Nomenclature: Schematic component symbols should be drawn with the appropriate amount of internal detail so that the schematics will clearly show the operation of the circuit. This information might consist of analog and digital, power supply and CPU connections. A good place to find these details is the component data sheet. Showing components as blocks with no internal details should only be resorted to when a component is so large or generic that the internal information is of minimal use or confusing. An example might be a very large CPU or FPGA. Even in that case, ideally, symbols should be designed so that they flow with inputs on the left, outputs on the right, power supplies on top pointing up, the grounds on the bottom pointing down, and grouping of signals together in such a way so as to simplify and clarify the schematics. Schematic designers should not be afraid of having multiple schematic library parts for the same part, with the caveat that the quality of the library should not be compromised. The reason for this is that, depending on the schematic, it may make more sense for a particular pin of an IC to be on the right or the left. Within a single schematic, however, it is normally preferable to have all of the component schematic symbols the same for any particular part.

Component labels are typically laid out with the reference number (R1) on top, the component value (10 K, 10 uF, etc) in the middle and any notes such as 0.1%, ½ watt on the bottom and the same from left to right. Examples are shown in Figure 10.

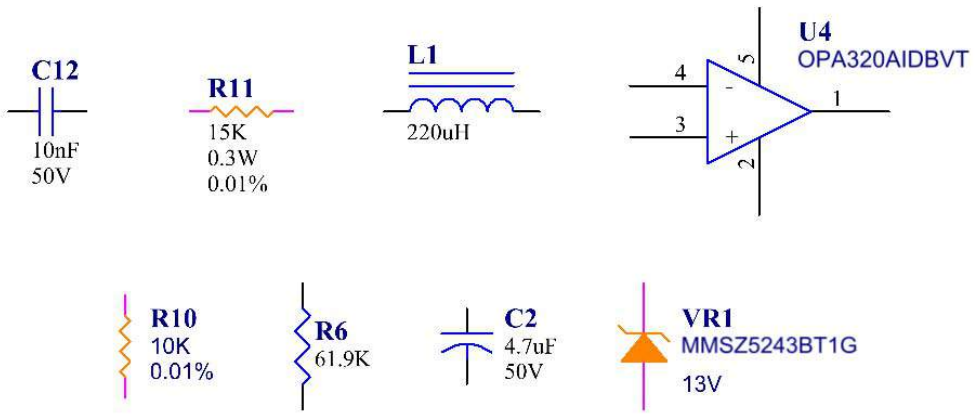


Figure 10 – Component Layouts

Notice that the nomenclature text is left justified, equally spaced vertically or horizontally. Reference numbers are on top, values next and voltage or tolerance on the bottom.

Pin names should be brief, intelligent descriptions, use underscores not spaces and begin with "N" or end with "*" for active low digital signals.

Schematic Component Libraries: The reuse of schematic component symbols and PCB footprints can greatly affect the quality and cost of schematics. A company-wide library that is properly created and maintained can be a great benefit in providing accurate schematic symbols and associated footprints. Reused library symbols can become a valuable asset in a design group library once they have are properly documented, tested and verified.

Schematic Fundamental Checklist:

1) Input range voltages should always be specified for power inputs and current levels.
2) All input and output signals leaving the board should be clearly and descriptively labeled.
3) High current traces above 0.3 amps should be labeled and indicated with bolder lines.
4) High voltage circuits should be labeled to make the design rules check work correctly.
5) …

Use of Color on Schematics: Schematics are almost always drawn in color, making them easier to see and understand on modern eCAD computer screens. This is a great improvement from the days of all black or blue schematics done in pencil on vellum and copied on a blue print machine. However, some customers may still require the final archive copy of schematics to be in black and white in order to correctly copy them on black/white copiers without losing information. In the design phase most engineers prefer the use of color pdf files to review since color is much easier to read and can be used to show circuit concepts. PDFs are also easier to email to a range of people for their review as they may not all have the same eCAD software. A well-known example of the need for color to speed up visual searches and increase clarity is the Washington DC metro map as referred to in the article "10 Reasons to use Color"[5]. In Figure 11 it is compared to a gray scale version to demonstrate the clarity that color provides.

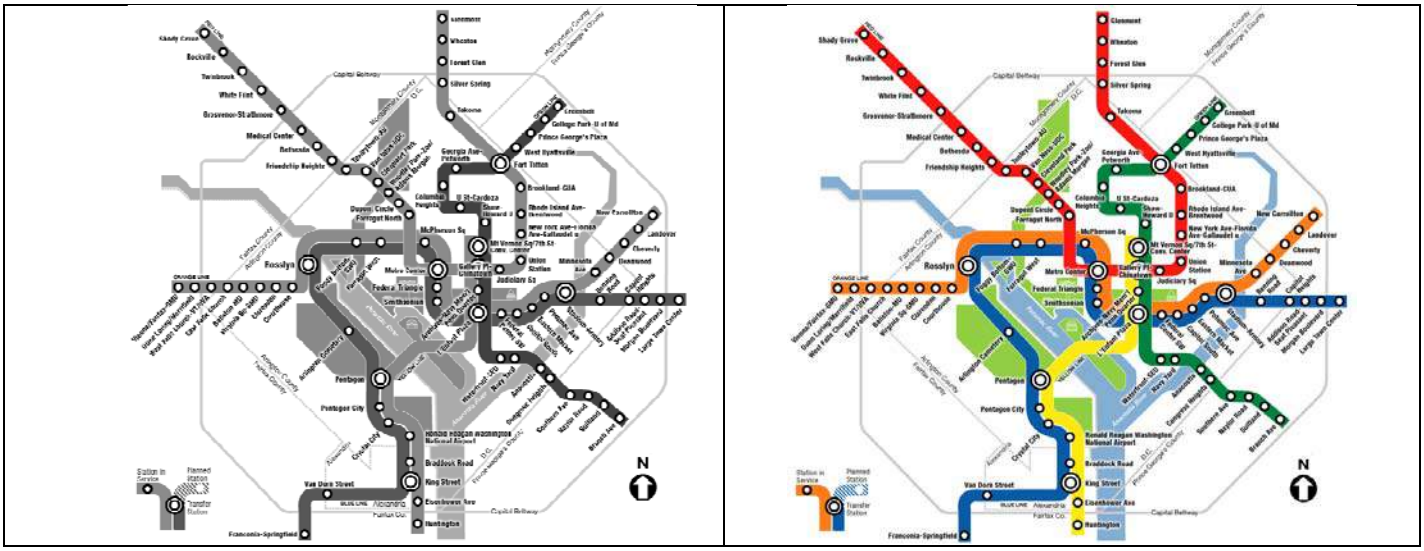


Figure 11 – Black and White versus Color

Schematic Quality: You can often measure the quality of schematics and sometimes the design before you get into the details. A color pdf of the schematics is a very effective tool to communicate to the 10 or more people described in the beginning of this article exactly how a circuit will work and what level of confidence they can have in the design. The following questions are some possible ways to evaluate the state and quality of a design:

1) Are the title block, revision history and notes complete and correct?
2) Do the schematics and BOM appear to be complete and correct upon first glance?
3) Are the operation and function of all circuits clear with little explanation?
4) How quickly can the designer explain to other engineers how the circuit works? Would 5 minutes/page be reasonable for simple designs?
5) Does the schematic pass a DRC (design rule check)?
6) Does the schematic document that it has been reviewed and approved by anyone other than the author?
7) Are the schematics artfully drawn in a way that shows how the circuit works?
8) Are the fonts, line connections, component symbols, nomenclature, notes, and circuit layouts consistent from page to page?

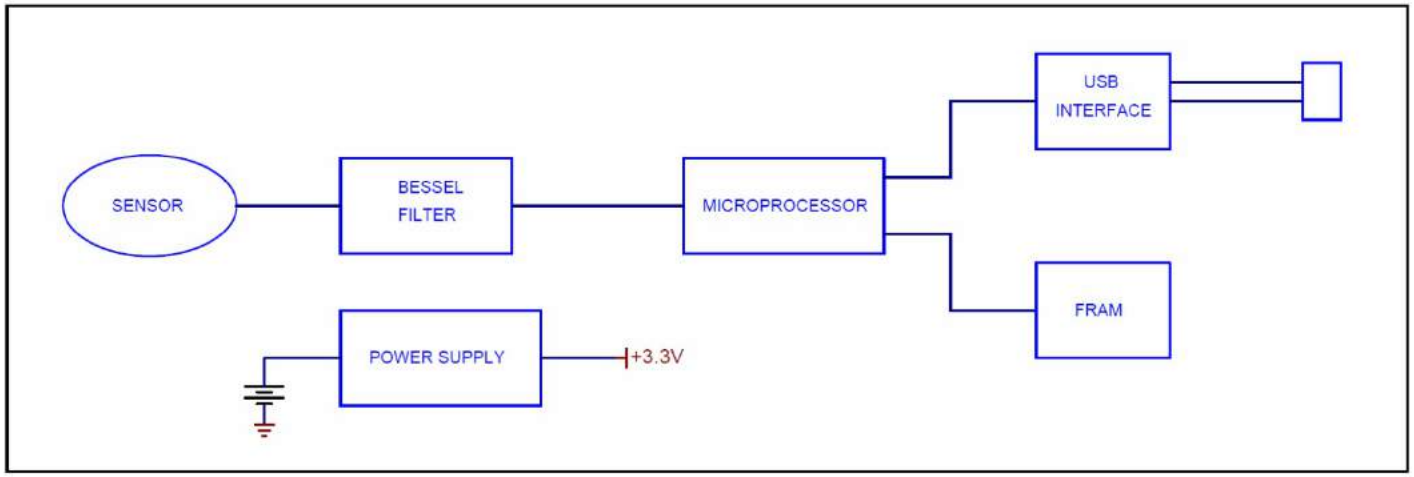
Conclusions: Paying close attention to the aesthetic and functional quality of schematics can greatly improve the quality of an electronics engineering project and reduce the cost and schedule. In the modern world of eCAD we say that if a schematic is correct then the BOM will be correct and the PCB layout will at least be connected correctly. With good enough schematic notes and an experienced PCB layout designer then the component placement and critical routing can also be directed by the schematics. Schematics are a good area to invest in to improve the quality and productivity of an electronics engineering department.

References:

1. IPC-2612-2010 Sectional Requirements for Electronics Diagramming Documentation (Schematics and Logic Descriptions)
2. http://electronics.stackexchange.com/questions/28251/rules-and-guidelines-for-drawing-good-schematics
3. http://opencircuitdesign.com/xcircuit/goodschem/goodschem.html
4. https://www.k-state.edu/edl/docs/pubs/technical-resources/Technote8.pdf
5. http://community.cadence.com/cadence_blogs_8/b/pcb/archive/2009/04/01/what-s-good-about-schematic-drawing-standards
6. http://understandinggraphics.com/design/10-reasons-to-use-color/

REVISIONS				
REV	DESCRIPTION	DATE	CHANGED	APPROVED
A	Initial design	05 JUL 16	Martin Co. (JK)	J. Martin
B	Update transducer filter circuit to 100Hz.	12 DEC 16	Martin Co. (JK)	J. Martin

Revision list gives a quick view of design history.



Block diagrams can provide a quick overview of the design concept.

Notes like these can avoid having to place additional information on every component.

All resistors are surface-mount thick-film unless otherwise specified.

All ceramic capacitors and X7R types unless otherwise specified.

Specifications, instructions, or other information can be added to the schematic as needed.

Specifications

Operating temperature range: 0 - 70°C

Battery input range: 6 - 15VDC

Typical operating current: less than 12mA.

All components and board must be RoHS compliant

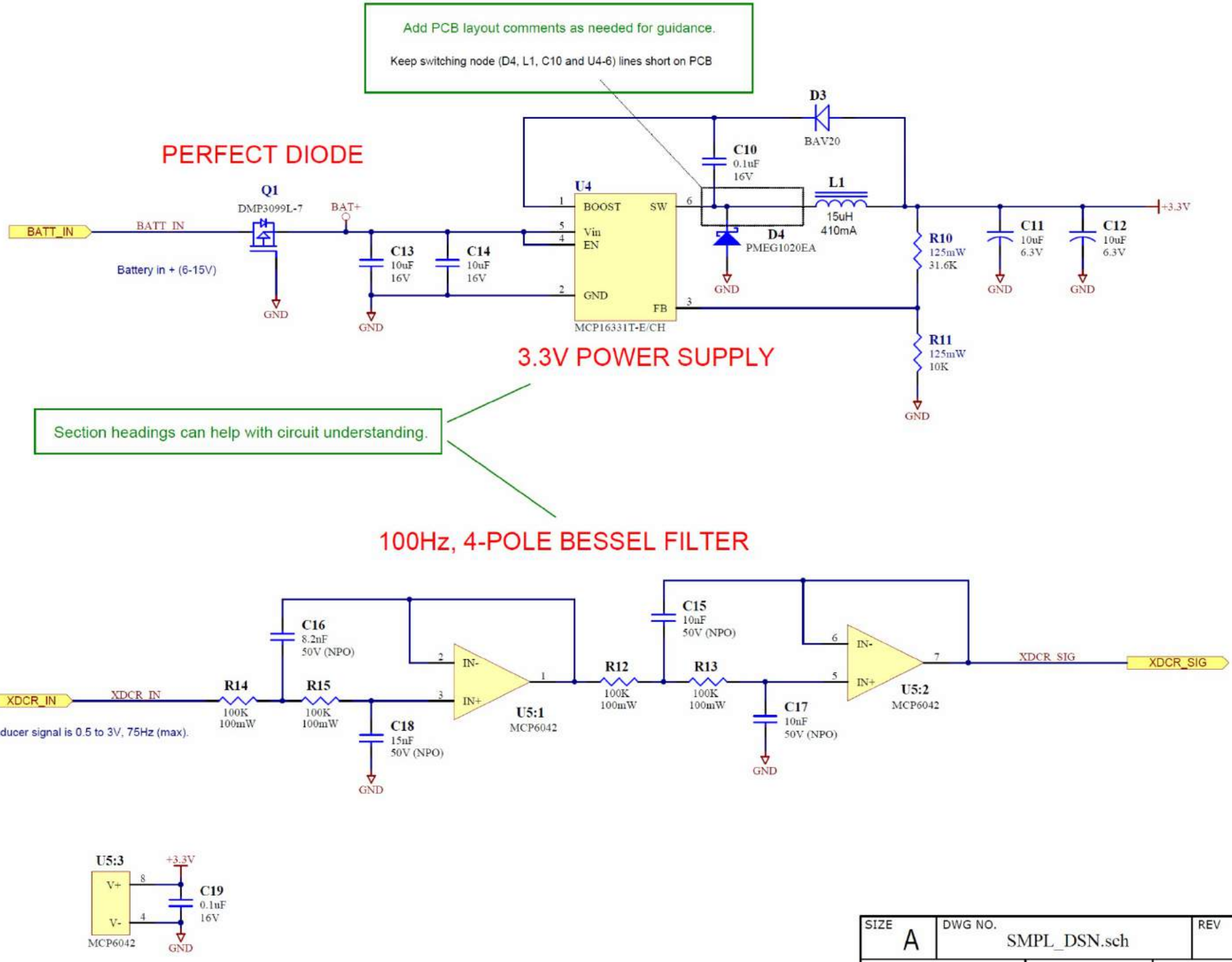
MARTIN COMPANY

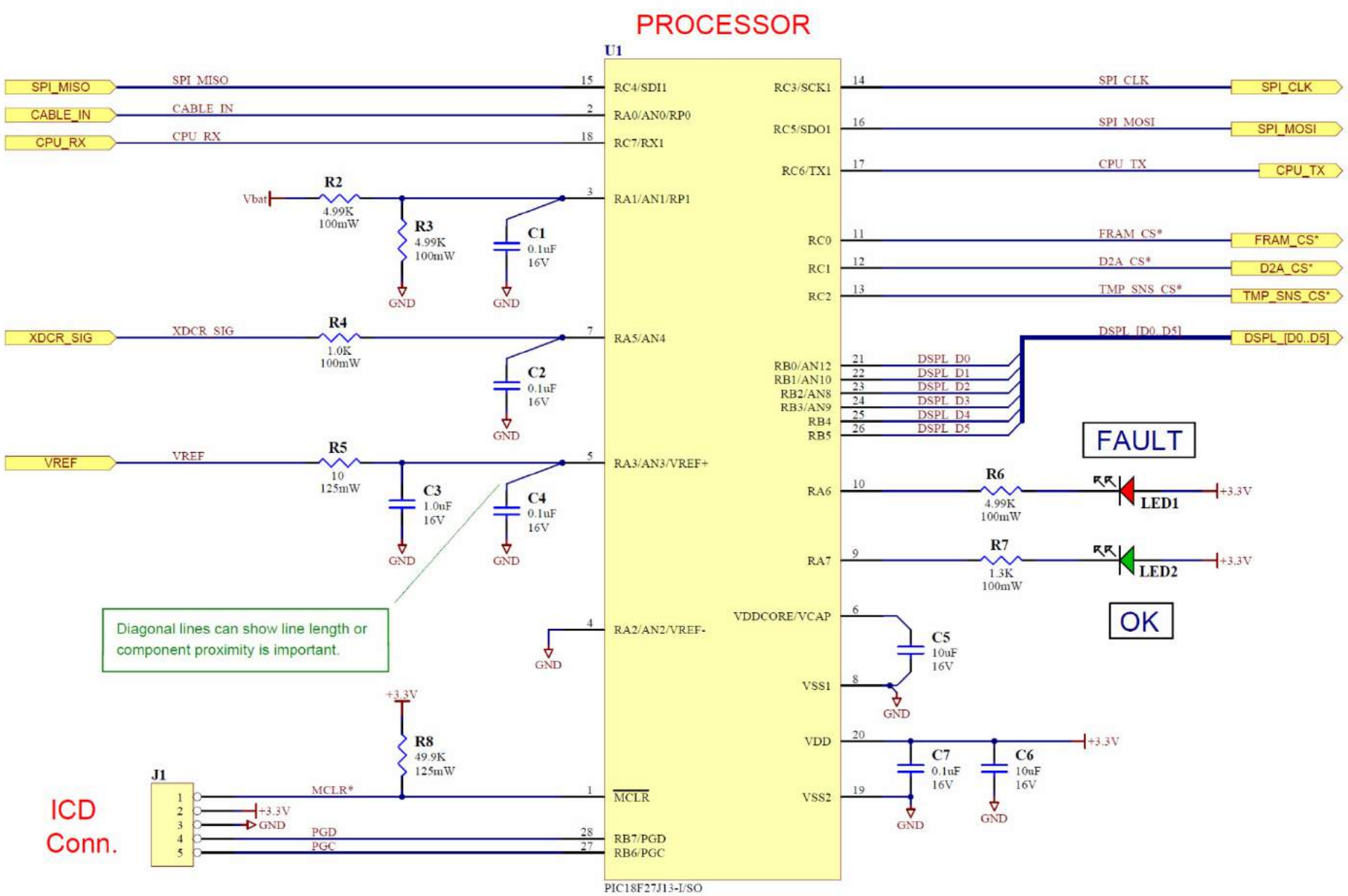
Martin Company
5330 Reading Road
Rosenberg, TX 77471

Data Acquisition System

SIZE	DWG NO.	REV
A	SMPL_DSN.sch	B

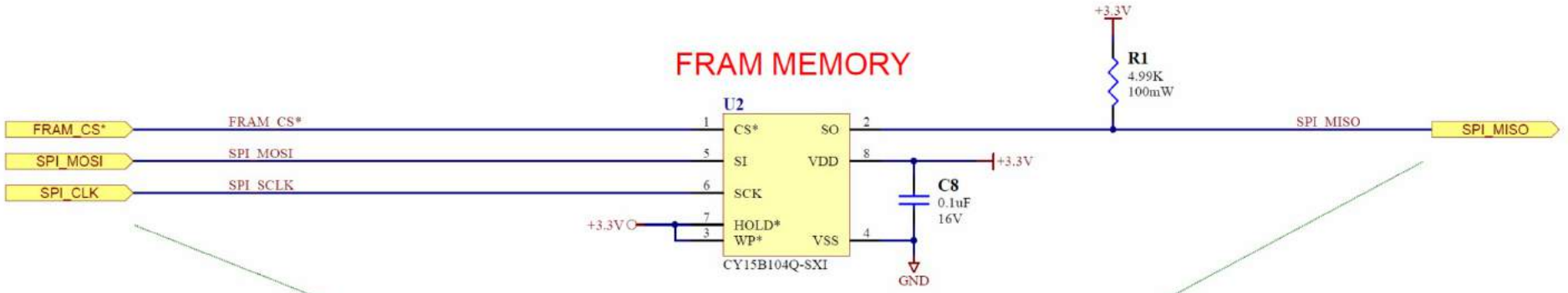
Approved by:	DRAWN BY:	DATE:	SHEET
J. MARTIN	Martin Co. (JK)	05 JUL 16	1 of 4


Add PCB layout comments as needed for guidance.
Keep switching node (D4, L1, C10 and U4-6) lines short on PCB
PERFECT DIODE
D3
BAV20
C10
0.1uF
16V
L1
15uH
410mA
Q1
DMP3099L-7
BAT+
BATT_IN
BATT_IN
Battery in + (6-15V)
U4
BOOST
SW
Vin
EN
GND
FB
MCP16331T-E/CH
D4
PMEG1020EA
C13
10uF
16V
C14
10uF
16V
R10
125mW
31.6K
C11
10uF
6.3V
C12
10uF
6.3V
+3.3V
R11
125mW
10K
GND
3.3V POWER SUPPLY
Section headings can help with circuit understanding.
100Hz, 4-POLE BESSEL FILTER
C16
8.2nF
50V (NPO)
C15
10nF
50V (NPO)
XDCR_IN
XDCR_IN
Transducer signal is 0.5 to 3V, 75Hz (max).
R14
100K
100mW
R15
100K
100mW
C18
15nF
50V (NPO)
U5:1
MCP6042
R12
100K
100mW
R13
100K
100mW
C17
10nF
50V (NPO)
U5:2
MCP6042
XDCR_SIG
XDCR_SIG
U5:3
V+
V-
MCP6042
C19
0.1uF
16V
SIZE
A
DWG NO.
SMPL_DSN.sch
REV
B
DRAWN BY:
Martin Co. (JK)
DATE:
05 JUL 16
SHEET
2 of 4



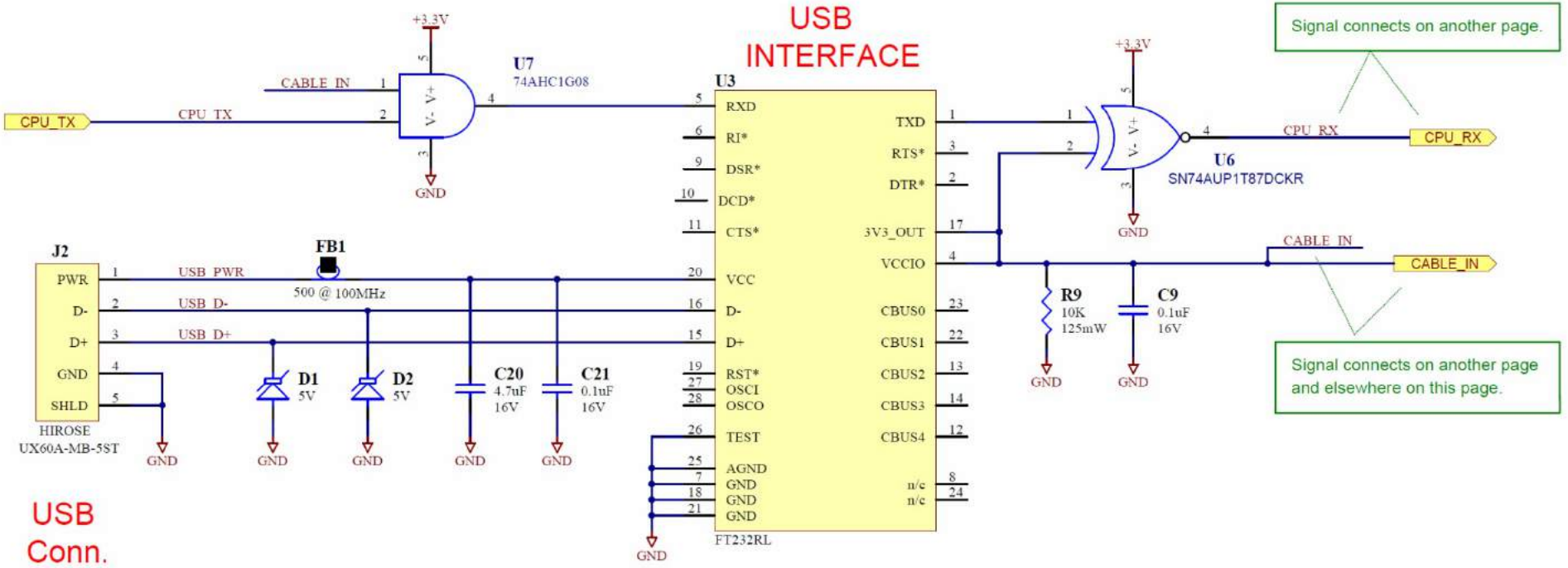
SIZE	DWG NO.	REV
A	SMPL_DSN.sch	B
DRAWN BY: Martin Co. (JK)	DATE: 05 JUL 16	SHEET 3 of 4

FRAM MEMORY



When possible, inputs should be on the left side and outputs on the right hand side.

USB INTERFACE



Signal connects on another page.

Signal connects on another page and elsewhere on this page.

USB Conn.

SIZE	DWG NO.	REV
A	SMPL_DSN.sch	B
DRAWN BY: Martin Co. (JK)	DATE: 05 JUL 16	SHEET 4 of 4